# Janet Vorobyeva

janet.vorobyeva@gmail.com • 347-603-3315

## EDUCATION

**UC San Diego** *Fall 2023 – Present*
- PhD in Computer Science
- Focus: Computer Architecture / Systems

**Stony Brook University** *2015 – 2020*
- MS in Computer Science GPA: 3.93
- BS (Honors) in Computer Science and Mathematics, Minor in Electrical Engineering GPA: 3.70

## WORK EXPERIENCE

**Graduate Student Researcher - UC San Diego** *Fall 2023 – Present*
- Research in CPU Architecture: Speculative Execution / Branch Predictors
- Research in Sustainable Computing and Low-Power Embedded Computing

**Software Developer - Grist Labs** *Summer 2023*
- Frontend developer for an in-browser spreadsheet application
- Untangled a long-standing constraint allowing bidirectional linking/updating of data views

**Computer Science Teacher – Stuyvesant High School** *Spring 2022*
- Taught 3 classes daily of introductory Python, and 2 of Java with Processing (150 students)

**Cybersecurity Researcher – Sandia National Labs** *2020 – 2022*
- Integrated a virtual-memory system into the "SST" CPU simulator (sst-simulator.org)
- Built tooling using write-optimized data structures to rapidly index high-volume network logs, yielding ~100x improvement in query times (see Vorobyeva et. al, 2022)
- Theory work on external-memory / write-optimized / data-oblivious data structures.
- (Worked first year as a graduate student researcher, second year as full-time employee)

**System Administrator Student Assistant – Stony Brook University** *2016 – 2019*
- Maintained the Seawulf HPC cluster, consisting of >150 centOS Machines
- Debugged HPC cluster software installations, network configurations, hardware issues

**Software Developer Intern – Grist Labs** *2017 – 2018*
- Implemented a dynamic scroll module for displaying large spreadsheets in a browser
- Profiled and optimized backend performance (Node.js/Python/SQL)

## PUBLICATIONS


- **Vorobyeva J.**, Delayo D.R., Bender M.A., Farach-Colton M., Pandey P., Phillips C.A., Singh S., Thomas E.D., Kroeger T.M.. (2022) **Using Advanced Data Structures to Enable Responsive Security Monitoring**. *Cluster Computing*
- Bender, M.A., Bhattacharjee, A., Conway, A., Farach-Colton, M., Johnson, R., Kannan, S., Kuszmaul, W., Mukherjee, N., Porter, D.E., Tagliavini, G., **Vorobyeva, J.**, & West, E. (2021). **Paging and the Address-Translation Problem**. *Proceedings of the 33rd ACM Symposium on Parallelism in Algorithms and Architectures*

## TECHNICAL SKILLS

Fluent in C, Python, JavaScript/Typescript
Experienced with Git, and Linux system administration
Proficient with LaTeX, NumPy/pandas/Matplotlib, C++
Some experience with HPC, Embedded systems, Rust, CUDA, Verilog, Perl

## NOTABLE COURSEWORK

**Embedded Networking:** Worked with bluetooth (BLE), 802.15.4 (Thread), WiFi, and LoRa networking on a Nordic nRF52840 embedded platform
**Computer Architecture:** Built a fully-forwarded and pipelined RISC-V CPU in Verilog with caches, virtual memory, and trap-handling
**Distributed Systems:** Implemented multi-threaded Raft consensus algorithm; built a sharded fault-tolerant key-value store on top of it
**Operating Systems:** Modified Linux kernel scheduler; added features to /proc
**Computational Geometry:** Studied algorithms for convex hulls, triangulations, etc; spatial data structures for point location, ranges. Implemented interactive voronoi-graph visualization (see Projects)

## NOTABLE PROJECTS

**CP/M Low Power Sensor:** An energy-harvesting sensor node able to run on 150uW of input power. I designed and assembled a custom PCB, and integrated a low-power microcontroller (Apollo3), an energy-harvesting IC, and a LoRa radio. (course project)
https://github.com/jvorob/cpm-firmware

**SUBLEQ Assembler / FORTH:** A personal project to bootstrap software from scratch for a home-brewed CPU architecture; starting with raw machine code, to writing an assembler, to a high-level language (FORTH) with disassembler, debugger, interactive REPL, stack introspection, etc.
https://github.com/jvorob/subleq-bootstrap

**Interactive Voronoi Tessellation:** Implementation of a doubly-connected-edge-list data structure, used to build an interactive voronoi diagram; written in Typescript. (course project)
https://jvorob.github.io/projects/voronoi/

**Prolog Interpreter:** Simple Prolog interpreter, written in Python
https://github.com/jvorob/jpl

**FORSH:** FORTH interpreter and virtual terminal written for a 6502 CPU emulator
https://github.com/jvorob/6502js

**Tron Cellular Automaton:** Implementation of the tron automaton
jvorob.github.io/projects/tron